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Original Article

Current THD Mitigation in a D-STATCOM via Reactive Power Set-Point Adaptation under DC-Link Capacitance Derating

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Abstract

In D-STATCOM (Distribution Static Synchronous Compensator) systems, the harmonic quality of the injected current is strongly affected by several operational and structural parameters, such as the achievable compensation level, modulation strategy, DC-link energy storage, and the characteristics of the AC-side filters. Among these elements, DC-link capacitors represent one of the most failure-prone components in power electronic converters due to aging effects, partial cell degradation, and protection-device malfunctions within capacitor banks. Such degradations modify the effective DC-link capacitance, leading to increased voltage ripple, constrained modulation capability, and a subsequent rise in current harmonic distortion at the point of common coupling (PCC), ultimately deteriorating grid power quality. To mitigate this issue, this paper introduces a supplementary adaptation scheme integrated as a secondary control layer into the conventional multi-loop control architecture. Instead of modifying the primary current and voltage controllers, the proposed approach dynamically adjusts the reactive power reference, thereby indirectly constraining the current THD within permissible limits. The method operates in steady-state conditions and remains compatible with existing control frameworks. Both simulation results and hardware-in-the-loop validations confirm that the proposed adaptation strategy effectively suppresses harmonic distortion and improves grid power quality, even under significant DC-link capacitance reduction.

Keywords: D-STATCOM, DC-link capacitor derating, Supplementary adaptation scheme, Current THD mitigation, Fault-tolerant control

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LIST OF SYMBOLS AND ABBREVIATIONS

P	*Exchange active power*
Q	*Exchange reactive power;*
V_t	*Terminal voltage of the voltage source converter*
V_{td}	*direct component of V_t in dq-frame*
V_{tq}	*quadrature component of V_t in dq-frame*
V_s	*Network voltage*
V_{sd}	*direct component of V_s in dq-frame*
V_{sq}	*quadrature component of V_s in dq-frame*
i	*AC-side current*
i_d	*direct component of i in dq-frame*
i_q	*quadrature component of i in dq-frame*
L	*AC-side coupling inductance*
R	*AC-side coupling resistance*
ω	*Angular frequency*
i_d^*	*Reference signal of i_d ;*
i_q^*	*Reference signal of i_q*
Q^*	*Reference signal of Q*
m	*Modulation index*
V_{dc}	*DC-link voltage*
V_{dc}^*,	*Reference signal of V_{dc}*
i_{dc}	*DC-link current*
C_{dc}	*Equivalent capacitance of the DC-link capacitor bank*
Δi_c	*Variation of the DC-link current*
f_{sw}	*Switching frequency*
f_n	*Network frequency*
ΔV_{dc}	*DC-link voltage ripple*
$i_{peak,dc}$	*Maximum of i_{dc}*
m_g	*Modulation index in no-load operation*
Δm	*Difference between operational modulation index and m_g*
Q_N^*	*Corrected Q^* generated by the adaptation mechanism*
s_q	*Detection signal identifying sudden changes in Q^**
Q_{N1}^*	*Instantaneous Q_N^**
Q_{N0}^*	*Previous Q_N^**
THD_i	*AC-side current THD*
Q_{flag}	*Time flag designating dynamic or static sequence in adaptation mechanism*
THD_{flaq}	*Time flag designating the THD regulation in adaptation mechanism*

1. INTRODUCTION

The increasing penetration of nonlinear and reactive loads in modern power systems has intensified concerns regarding operational stability, thermal constraints, and power quality across generation, transmission, and distribution levels [1–3]. In response to these challenges, advanced power electronic solutions, including Flexible AC Transmission Systems (FACTS) and custom power devices, have been widely adopted to enhance system controllability and

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performance. Among these solutions, the distribution static synchronous compensator (D-STATCOM) has emerged as an effective shunt-connected device for distribution networks, offering fast and flexible reactive power control to regulate voltage, mitigate flicker, and improve power quality at the point of common coupling (PCC) [4–6].

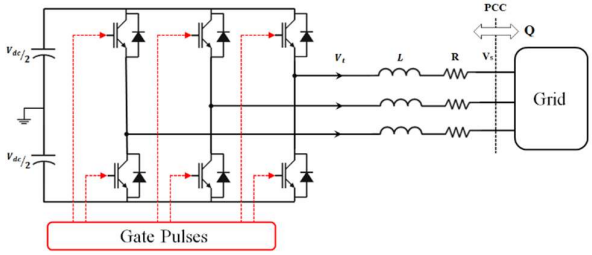


Fig. 1. Configuration of the D-STATCOM

As depicted in Fig. 1, a D-STATCOM is typically implemented using a voltage-source converter (VSC) interfaced with the PCC through an inductive coupling filter. By dynamically controlling the converter output voltage, the D-STATCOM can either inject or absorb reactive power, depending on the VAr requirements imposed by the connected load. The achievable compensation performance of the device is closely linked to several design and operating parameters, including the DC-link voltage level, the effective capacitance of the DC-link energy storage, the characteristics of the switching devices, and the impedance of the AC-side filter [7–8]. Deviations from nominal values in any of these parameters—whether caused by component aging, faults, or operational stresses—can degrade the compensation capability of the D-STATCOM, thereby compromising voltage regulation, system stability, and power quality at the PCC [9].

Among the aforementioned parameters, the DC-link capacitor bank (CB) plays a particularly critical role, especially under high loading and maximum compensation conditions. The DC-link capacitance directly influences the voltage ripple magnitude, the transient response of the converter, and the upper limit of reactive power support. Consequently, variations in capacitance have a pronounced impact on both the dynamic behavior of the D-STATCOM and the quality of power delivered to the grid. In practical designs, the DC-link capacitor size is intentionally constrained due to safety, cost, and reliability considerations [10]. Furthermore, the DC-link voltage dynamics inherently exhibit a right-half-plane (RHP) zero, implying that a reduction in capacitance may introduce adverse dynamic effects, including reduced stability margins, excitation of unstable modes, and unintended activation of protection mechanisms.

To improve the robustness of power electronic converters against DC-link capacitor degradation and failure, prior research has addressed this issue from multiple perspectives, including analytical modeling and physical interpretation of failure mechanisms [9], [12], as well as enhanced design methodologies and validation procedures [13–14] and the control and monitoring of the DC-link CB [15-17].

Analytical studies grounded in physical modeling primarily investigate capacitor degradation modes and failure mechanisms to predict the expected lifetime of DC-link capacitors under electrical and thermal stress conditions [9]. In parallel, design- and verification-oriented research emphasizes the development of structurally robust capacitor-bank (CB) configurations aimed at improving system survivability during fault events [13–14]. While these studies mainly address DC-link reliability prior to commissioning and normal operation, real-time control and monitoring strategies focus on the behavior of the system during online operation [9]. Monitoring-based approaches rely on estimating key electrical indicators to anticipate short-term performance variations, whereas control-oriented methods aim to preserve converter operability near nominal conditions through fault-tolerant control design.

A variety of nonlinear and robust control techniques have been reported for D-STATCOM applications, including formulations based on nonlinear differential–algebraic equations [18], feedback linearization (FL) [19], passivity-based control schemes [20], and hybrid strategies combining H∞ control with FL [21]. Although these approaches can satisfy general control objectives, they neither explicitly address DC-link capacitor degradation nor consider capacitance-reduction scenarios. Moreover, their implementation often introduces additional computational and structural complexity into the control system.

A decrease in DC-link capacitance can significantly restrict the operational margin of a D-STATCOM and may activate protective mechanisms that force the compensator to disconnect from the PCC. Under such circumstances, the upstream grid must directly supply the reactive power demanded by sensitive loads, which can negatively affect voltage regulation and overall power quality. These consequences highlight the necessity of control solutions capable of sustaining acceptable system performance during DC-link capacitor degradation while alleviating stress on the distribution network.

In response to this requirement, this paper develops a control strategy that determines an optimal operating region for a D-STATCOM subjected to reduced DC-link capacitance. The proposed algorithm continuously evaluates power-quality indicators—particularly the AC current THD at the PCC—and accordingly regulates the reactive power operating point to maintain effective compensation under faulty conditions.

It should be emphasized that the novelty resides in introducing a supervisory THD-constrained reactive power adaptation layer that operates without modifying the existing cascaded control structure. This implementation-oriented characteristic enables straightforward integration into already deployed D-STATCOM systems while enhancing robustness against DC-link capacitance degradation.

The remainder of the paper is organized as follows. Section II presents the D-STATCOM model and analyzes the impact of DC-link capacitance reduction relative to normal operation, followed by the formulation of an adaptive

optimal strategy that satisfies power-quality constraints with minimal burden on the grid. Sections III and IV validate the proposed method through simulation studies and hardware-in-the-loop experiments, respectively. Finally, Section V concludes the paper.

2. Steady-State Analysis Under DC-Link Capacitance Derating

The power interaction between the D-STATCOM and the utility grid, depicted in Fig. 1, is analyzed at the PCC using a synchronous dq-frame representation, through which the corresponding active and reactive power terms are obtained as follows [22–24]:

$$P = \frac{3}{2}(V_{sd}i_d + V_{sq}i_q) \tag{1}$$

$$Q = \frac{3}{2}(V_{sq}i_d - V_{sd}i_q) \tag{2}$$

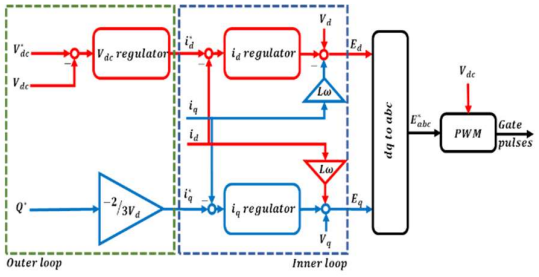


Fig. 2. Control System Structure

In a D-STATCOM, the control system is required to regulate the voltage at the VSC's terminals, V_t by generating appropriate voltage reference signals for the pulse-width modulation (PWM) units. In a dq-frame, V_{td} and V_{tq} are determined as follows:

$$V_{td} = L\frac{di_d}{dt} + Ri_d - L\omega i_q + V_{sd} \tag{3}$$

$$V_{tq} = L\frac{di_q}{dt} + Ri_q - L\omega i_d \tag{4}$$

where L, R, and ω are coupling inductance, coupling resistance, and angular frequency. Fig. 2 illustrates the conventional control architecture employed in a D-STATCOM. In the cascaded framework, DC-link voltage and reactive power are regulated by the outer loop, whereas the inner loop governs the dq-axis currents to generate appropriate PWM control actions.

$$i_d^* = 0 \tag{5}$$

$$i_q^* = -\frac{2}{3V_{sd}}Q^* \tag{6}$$

Moreover, under steady-state operating conditions, i_d and i_q track their respective reference values, and consequently V_{td} and V_{tq} can be expressed as follows:

$$V_{td} = V_{sd} + \frac{2L\omega}{3V_{sd}}Q^* \tag{7}$$

$$V_{tq} = \frac{-2R}{3V_{sd}}Q^* \tag{8}$$

Accordingly, the steady-state modulation index can be determined as follows:

$$m = \frac{4}{3V_{dc}^*V_{sd}}\sqrt{(1.5V_{sd}^2 + L\omega Q^*)^2 + R^2} \tag{9}$$

Since, in practical applications, $L\omega$ is significantly larger than R, the resistance term can be neglected, and (9) can be rewritten as:

$$m = \frac{6V_{sd}^2 + 4L\omega Q^*}{3\,V_{dc}^*V_{sd}} \tag{10}$$

According to (10), the modulation index depends on the reactive power reference and the DC-link voltage reference.

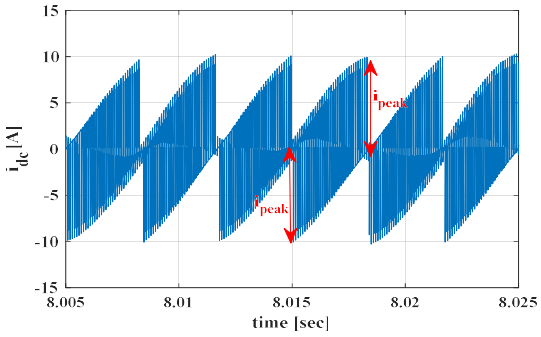


Fig. 3. DC-Link Current Characteristics at Grid Frequency

It should be noted that (10) yields higher accuracy when the actual DC-link voltage, V_{dc} is used instead of its reference value, particularly in the presence of noticeable DC-link voltage ripple. The allowable magnitude of the DC-link voltage ripple is typically specified during the design stage and is commonly limited to less than 0.05 V_{dc}^*. This parameter plays a significant role in determining the required size of the DC-link capacitor bank. Under Var compensation and assuming steady-state and ideal operating conditions, the DC-link current can be expressed as follows:

$$i_{dc} = C_{dc}\frac{dV_{dc}}{dt} \tag{11}$$

where i_{dc} and C_{dc} denote the DC-link current and the equivalent capacitance of the capacitor bank, respectively. As illustrated in Fig. 3, the dominant frequency component of the DC-link current is six times the grid frequency. In this inverter topology, the variation of the DC-link current reaches its maximum value, $i_{peak,dc}$, in half of a switching period [22-24]. Under VAr compensation and steady-state operating conditions, the peak value of the AC current is equal to the reactive current component (reactive current reference). Accordingly, the relationship between the DC-link characteristics and the required reactive power can be expressed as follows:

$$i_c = \frac{C_{dc}\Delta V_{dc}}{T_{sw}/2} \xrightarrow{i_{peak,dc}=i_q^*} i_q^* = 2C_{dc}f_{sw}\Delta V_{dc} \xrightarrow{(6)} Q^* = 3V_{sd}f_{sw}C_{dc}\Delta V_{dc} \quad (12)$$

where f_{sw} denotes the switching frequency. According to (12), V_{sd} and f_{sw} are constant parameters; therefore, the reactive power reference, Q^* depends on the capacitor bank capacitance and the DC-link voltage ripple. More specifically, Q^* proportional to the product multiplication of C_{dc} and ΔV_{dc}.

For a fixed value of Q^* degradation or failure of some capacitor units in the capacitor bank—due to aging, fuse malfunction, or cell failure—results in an increase in the DC-link voltage ripple. The DC-link voltage ripple is directly related to the AC-side current ripple and the resulting current THD; therefore, when it exceeds a specified allowable range, the current THD increases, leading to a deterioration of power quality compared to normal operating conditions [25–26].

Moreover, proportional–integral (PI) controllers are the most commonly employed control elements in the cascaded control structure shown in Fig. 2. These controllers are typically tuned based on nominal system parameters [27] and, as a result, their performance degrades when the capacitor bank capacitance (DCBC) deviates from its nominal value. Consequently, the development of an enhanced control strategy capable of preventing power quality deterioration—particularly in terms of current THD—becomes essential.

As indicated in (10) and (12), both the modulation index and the DC-link voltage ripple can be regulated through the reactive power reference Q^* under steady-state conditions. Accordingly, (13) can be derived by combining (10) and (12).

$$m = \frac{6V_{sd} + 12L\omega f_{sw}C_{dc}\Delta V_{dc}}{3V_{dc}^*} \quad (13)$$

Since V_{dc}^* and V_{sd} are constant, (13) can be rewritten as

$$\Delta m = m - m_g = \frac{4L\omega f_{sw}C_{dc}\Delta V_{dc}}{V_{dc}^*} \quad (14)$$

where $m_g = 2V_{sd}/V_{dc}^*$, which is a constant parameter. Under ideal operating conditions, the second term in (14) represents the increase or decrease of the modulation index relative to its nominal no-load value in order to supply the required reactive power Q^* at the PCC. This analysis indicates that higher values of Q^*, resulting from an increase in inductive loading at the PCC, lead to an increase in the modulation index through the associated rise in DC-link voltage ripple. This effect, in turn, increases the normalized AC-side current ripple and consequently elevates the current THD injected into the network at the PCC [28], [29]. Moreover, the occurrence of DC-link capacitor bank (DCBC) degradation under a constant compensation level further amplifies the DC-link voltage ripple, thereby worsening power quality indices, particularly the current THD.

It should also be noted that the modulation index must remain below the over-modulation region, as operation in this range distorts the AC voltage waveform at the VSC terminals and results in a substantial increase in the injected current THD. Such conditions typically arise when the D-STATCOM is forced to operate under overload scenarios. Without modifying the primary cascaded control structure shown in Fig. 2, this paper introduces a Supplementary adaptation scheme (SAS) integrated with the existing configuration to maintain the modulation index and DC-link voltage ripple within acceptable limits, thereby preventing further degradation of current THD.

As depicted in Fig. 4, the proposed SAS leaves the primary PI controllers unchanged and solely determines a new reactive power Q_N^* using Q^* and modulation index, DC-link voltage, and AC current THD, THD_i,

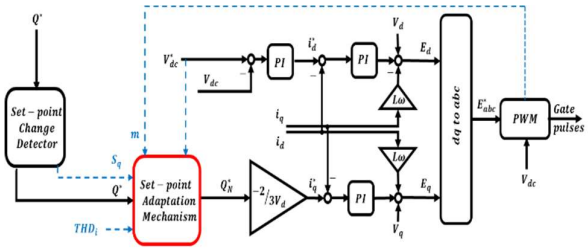


Fig. 4. Proposed Control Structure

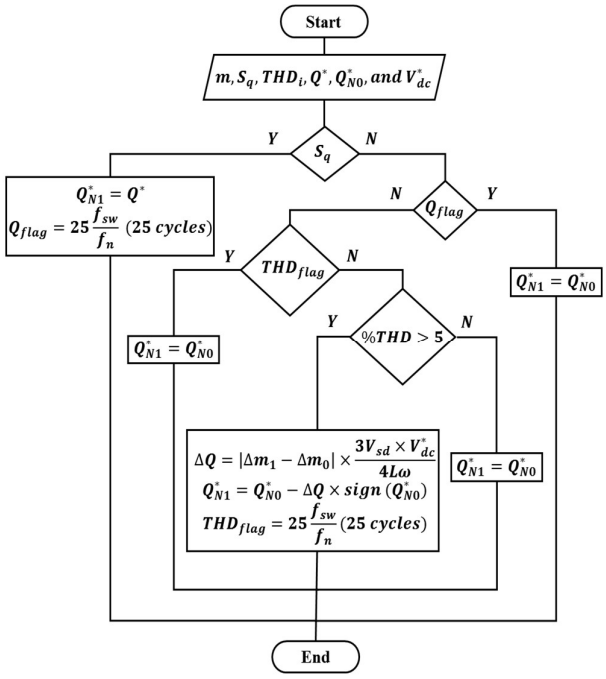


Fig. 5. Proposed Adaptation Mechanism

measurements. This upstream control layer operates based on steady-state system measurements and exhibits a slower dynamic response compared to the downstream control loops. From a steady-state perspective, (10) and (12)

indicate that the reactive power reference Q^* plays a pivotal role in the amount of THD_i through changing the $C_{dc}\Delta V_{dc}$ and m. When the measured current THD, THD_i, exceeds the predefined acceptable threshold during operation, the set-point adaptation mechanism adjusts the reactive power reference to a new value Q_N^* that is lower than Q^*, This reduction in the injected reactive power at the PCC decreases both the DC-link voltage ripple and the modulation index, thereby THD_i driving back into the admissible range. With the application of this adaptation mechanism, the upstream network supplies the reactive power difference between Q_N^* and Q^* to meet the load demand at the PCC. A smaller magnitude of $|Q_N^* - Q^*|$ is more desirable from a power quality perspective, as it reduces the stress imposed on the upstream network. If THD_i remains within the limits specified by the relevant standards, the adaptation mechanism does not modify the reactive power reference, and consequently $Q_N^* = Q^*$. Furthermore, since the D-STATCOM is required to exhibit fast dynamic response to supply the demanded reactive power during transient operating conditions, the proposed algorithm prioritizes this primary function. Accordingly, Q_N^* is temporarily set

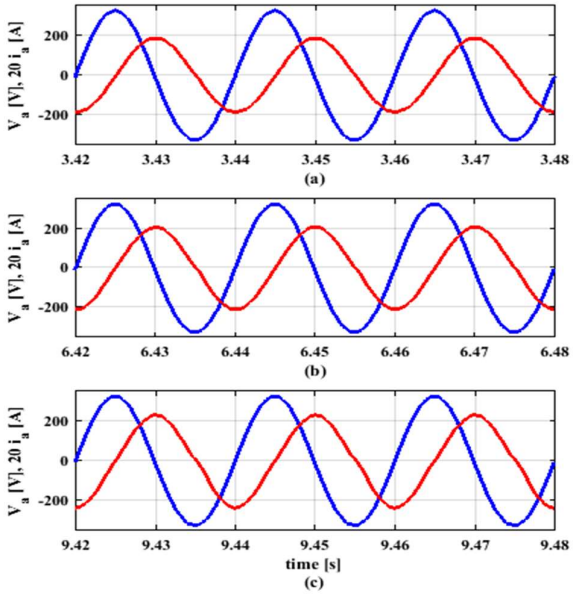


Fig. 6. Phase-a voltage and current waveforms under (a) 4.5 kVAr, (b) 5 kVAr, and (c) 5.5 kVAr operating conditions for the healthy scenario using the basic control structure shown in Fig. 2

equal to Q^* to avoid imposing abrupt disturbances on the network. This operating mode is enabled by the detection signal, s_q, applied to the adaptation mechanism. Once Q^* is updated, the detection block identifies this change and immediately generates a unit impulse at the s_q terminal, which is then applied to the adaptation block. Upon receiving this signal, the adaptation block temporarily suspends its operation and sets $Q_N^* = Q^*$ for a limited number of cycles (e.g., 25 cycles), even though the current THD may temporarily exceed the permissible range. This transient-priority override can be interpreted as a fault-tolerant and fault ride-through operating mode, ensuring that the D-STATCOM preserves fast dynamic response during abrupt reactive power

reference changes, while the THD-oriented corrective action is reactivated after a predefined delay. It should be noted that the adaptation procedure resumes its normal operation after the specified time interval. The flowchart of the set-point adaptation mechanism is shown in Fig. 5. To adjust Q_N^*, the proposed algorithm exploits the relationship between the modulation index and the reactive power reference Q^* as expressed in (10). Accordingly, this relationship can be rewritten as follows:

$$\Delta m = m - m_g = \frac{4L\omega Q^*}{3\,V_{dc}^* V_{sd}} \tag{15}$$

where m_g is a constant parameter defined in (14). Under steady-state operating conditions and for $s_q = 0$, the difference between m, obtained from the control system, and m_g, Δm_1, is computed, and then, the amount of expected Δm, Δm_0, also is determined by (15).

In the subsequent step, the absolute difference $|\Delta m_1 - \Delta m_0|$ is evaluated. Based on this value, the deviation of the required reactive power from its nominal reference, denoted as ΔQ^*, is calculated and subtracted from Q^*, to generate the updated reference Q_N^*. This new reference is applied to the control system for a predefined time interval, approximately 25 cycles (500 ms). If the resulting current THD_i, remains within acceptable limits, the adaptation mechanism retains this updated value of Q_N^*. Otherwise, the algorithm iteratively repeats its procedure to compute a revised reference, Q_{N1}^*, based on the previous value, until the THD_i constraint is satisfied.

The process of the adaptation mechanism is presented in Fig. 5. In this framework, Q_{flag} and THD_{flaq} are two control flags used to adjust the duration of the original reactive power set-point modification and the THD reduction operation, respectively. Furthermore, Q_{N0}^*, f_{sw}, and f_n denote the output of the adaptation mechanism at the previous sampling instant, the switching frequency, and the grid frequency, respectively.

Since the proposed adaptation mechanism operates as a supervisory outer layer acting solely on the reactive power reference, the inherent stability of the primary cascaded control loops remains unaffected. The adaptation process is activated only under steady-state conditions and operates at a slower time scale compared to the inner current control loops. Moreover, the reactive power adjustment is limited in magnitude and applied incrementally, thereby preventing abrupt reference variations and preserving closed-loop stability.

3. Numerical Assessment of the Proposed Control Strategy

The proposed control approach was evaluated and compared with the conventional control structure with MATLAB. In the simulation studies, a variable reactive load was assumed to be connected to a 400-V distribution network, while a 5-kVAr D-STATCOM was installed at the PCC to supply the required reactive power. Based on the full

compensation capability of the D-STATCOM and the imposed power quality requirements, the system parameters were designed according to [30] and are summarized in Table 1. To investigate the performance of the proposed control strategy in comparison with the primary control scheme, two operating scenarios were considered. In the first scenario, the inductive load begins to absorb 4.5 kVAr of reactive power from the network at t=1 s. Subsequently, the reactive power demand increases to 5 kVAr and 5.5 kVAr at t=4s and t=7s, respectively. In the second scenario, the reactive load follows the same variation as in the first case; however, it is assumed that half of the capacitors in one leg of the capacitor bank, as shown in Fig. 1, fail abruptly. As a result, the equivalent DC-link capacitance is reduced by approximately 33% compared with the first scenario. Throughout the remainder of this paper, the first and second scenarios are denoted as $\mathcal{H}_0$ (healthy) and $\mathcal{H}_1$ (faulty), respectively. For both operating conditions, the PI controller parameters were tuned based on the criteria reported in [27], and the corresponding values are listed in Table 2.

TABLE 1. Three Phase D-STATCOM System Parameters

Symbol	Value	Description
S_n	5kVA	Rated Power
V	400V	Nominal Bus Voltage
f	50Hz	Fundamental Frequency
f_{sw}	10kHz	Switching Frequency
V_{dc}	730V	DC-link Voltage
L	12.8mH	Inductance of AC Filter
C	150µF	Capacitance of DC-link

TABLE 2. Designed Controllers' Gains

Loop / Gain	i_d	i_q	V_{dc}
k_p	8	8	0.1
k_i	800	800	10

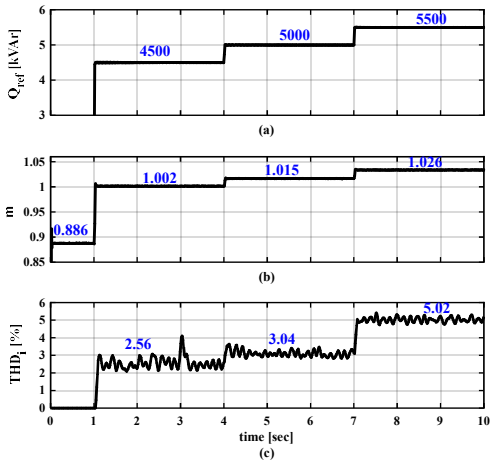


Fig. 7. (a) Reactive power reference; (b) modulation index; (c) THD_i; under healthy scenario and basic control structure shown in Fig. 2

As illustrated in Fig. 6, the voltage and current waveforms of phase a exhibit nearly pure sinusoidal shapes under the healthy operating scenario. This observation confirms that the THD levels of both voltage and current remain low and within the permissible limits, while the contribution of higher-order harmonic components in the injected reactive current is negligible compared to the fundamental component. This behavior is further verified in Fig. 7, where the current THD remains below the 5% limit for different compensation levels—namely under-full load (UFL), full load (FL), and over-full load (OFL), corresponding to 90%, 100%, and 110% of the nominal compensation rate, respectively—consistent with the IEEE Std. 519-2014 requirement for current harmonic distortion at the point of common coupling (PCC).

According to Fig. 7, the modulation index exceeds unity after t=4s. This observation indicates that, although the sinusoidal PWM operates in the over-modulation region during this interval, the power quality—particularly in terms of the current THD—remains within acceptable limits under Scenario 1. Moreover, operation in the over-modulation region without degradation of power quality indices contributes to a reduction in the switching losses of the D-STATCOM. The DC-link voltage profile is presented in Fig. 8, which demonstrates an increase in voltage ripple corresponding to variations in the reactive power reference.

To evaluate the effectiveness of the proposed method in mitigating the adverse impacts of a DC-link capacitor bank (DCBC) fault on the D-STATCOM, the conventional control structure shown in Fig. 2 is replaced with the proposed configuration illustrated in Fig. 4. Compared with the basic control scheme, the proposed approach reduces the amount of reactive power injected into the network in order to decrease the modulation index and, consequently, restore the current THD, to the permissible range. This behavior is clearly demonstrated in Figs. 12 and 13, which show that the adaptation mechanism lowers Q_N^* relative to the incoming reference Q^* applied to the adaptation block in Fig. 4.

More specifically, the proposed algorithm limits the reactive power compensation to an admissible level—here approximately 4114 VAr—at t=1.5s, t=4.5s, and t=7.5s. Figure 12 presents the D-STATCOM current waveforms over different time intervals and indicates that the currents become more sinusoidal when $s_q = 0$ and the adaptation mechanism actively adjusts the reactive power reference in accordance with the specified power quality requirements.

To avoid interference with the fast transient response of the primary control loops, the adaptation mechanism is temporarily suspended during abrupt variations of the reactive power reference, ensuring that dynamic compensation performance remains unaffected.

It is observed that the maximum reactive power reduction under the proposed adaptation mechanism is approximately 18% relative to the nominal 5 kVAr rating. This limited derating ensures compliance with IEEE 519 THD constraints while maintaining acceptable voltage regulation at the PCC under the tested operating conditions.

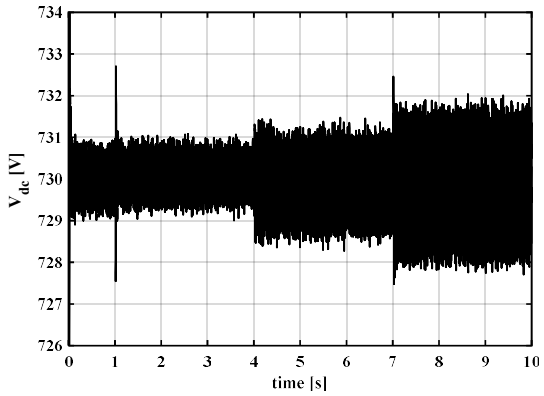


Fig. 8. DC-link voltage ripple under the healthy operating scenario using the basic control structure shown in Fig. 2

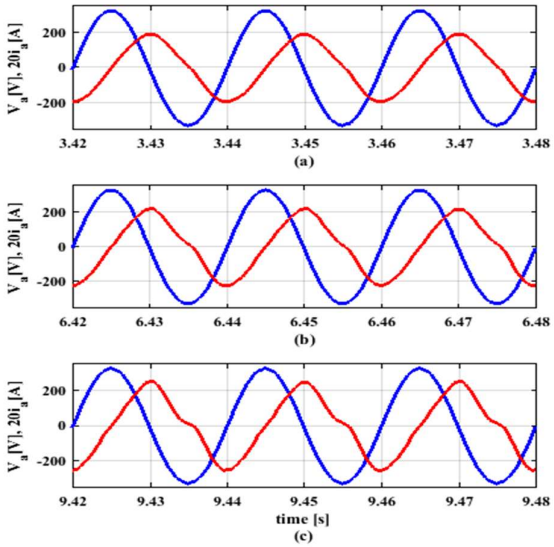


Fig. 9. Voltage and current waveforms of phase a under (a) 4.5 kVAr, (b) 5 kVAr, and (c) 5.5 kVAr operating conditions for the faulty scenario using the basic control structure shown in Fig. 2

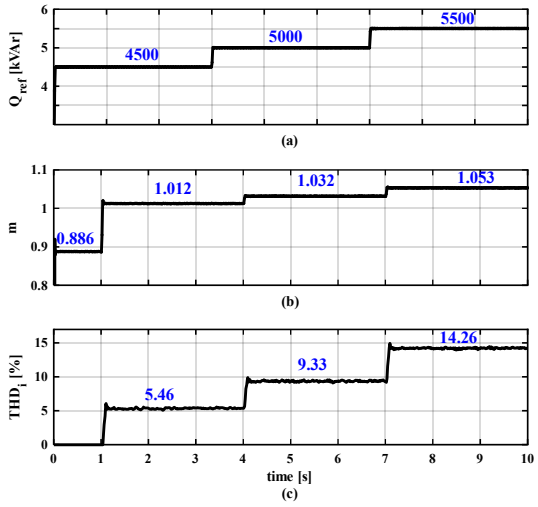


Fig. 10. (a) Reactive power reference; (b) modulation index; (c) THD_i; under a faulty scenario and basic control structure shown in Fig. 2.

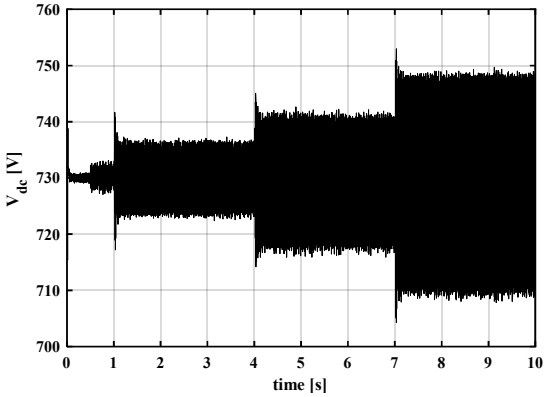


Fig. 11. DC-link voltage ripple under faulty scenario and basic control structure shown in Fig. 2.

Although the magnitude of $|Q_N^* - Q^*|$ becomes relatively large under the over-full-load (OFL) operating mode, the proposed method ensures that THD_i, remains within the acceptable system limits, i.e., below 5%. In addition, Fig. 13 illustrates that the adaptation mechanism temporarily overrides the original reactive power reference Q^* in the under-full-load (UFL), full-load (FL), and OFL compensation modes to promptly supply the required reactive power at the PCC and thereby prevent sudden disturbances to the network. Moreover, passive compensation elements such as switched capacitors and reactors are commonly installed in power networks to supply reactive power under steady-state operating conditions. By prioritizing the original reactive power reference Q^* at transition instants, the proposed algorithm provides sufficient time for the network to activate these passive elements and compensate the difference $|Q_N^* - Q^*|$ during the THD correction process. The proposed control strategy also reduces the DC-link voltage ripple at different compensation levels in order to regulate THD_i. This behavior is illustrated in Fig. 14, where the algorithm prevents the DC-link voltage ripple from exceeding the permissible range. It should be noted that this range is not explicitly imposed by the algorithm; rather, it emerges naturally as a consequence of the applied correction procedure, as can be intuitively observed.

4. Hardware-Based Verification

To experimentally validate the proposed approach, a 5-kVAr three-phase two-level D-STATCOM was designed and implemented, with its DC-link configuration shown in Fig. 2. The experimental setup is illustrated in Fig. 15, and the corresponding system parameters are summarized in Table 1. The control algorithm was implemented on a TMS320F28335 digital signal processor (DSP) operating at 150 MHz. To emulate DC-link capacitor bank faults and abrupt capacitance variations, a dedicated fault injection simulator was developed using an ATmega32 microcontroller. As depicted in Fig. 16, this simulator enables selective disconnection of capacitor units in both the positive and negative DC-link rails by issuing commands to relay contactors via a serial communication interface programmed in CodeVision AVR. Finally, the experimental

measurements were captured using a Hioki 3196 power quality analyzer and a Tektronix TDS2024C digital oscilloscope.

Similar to the simulation studies, the faulty operating condition is experimentally implemented by means of relay switches installed in the capacitor bank circuit shown in Fig. 16. Figure 17 illustrates the reactive power injected by the D-STATCOM into the network during steady-state operation, where the adaptation mechanism begins to modify the reactive power reference when $s_q = 0$. It can also be observed that the injected reactive power follows the original reference values when $s_q = 1$.

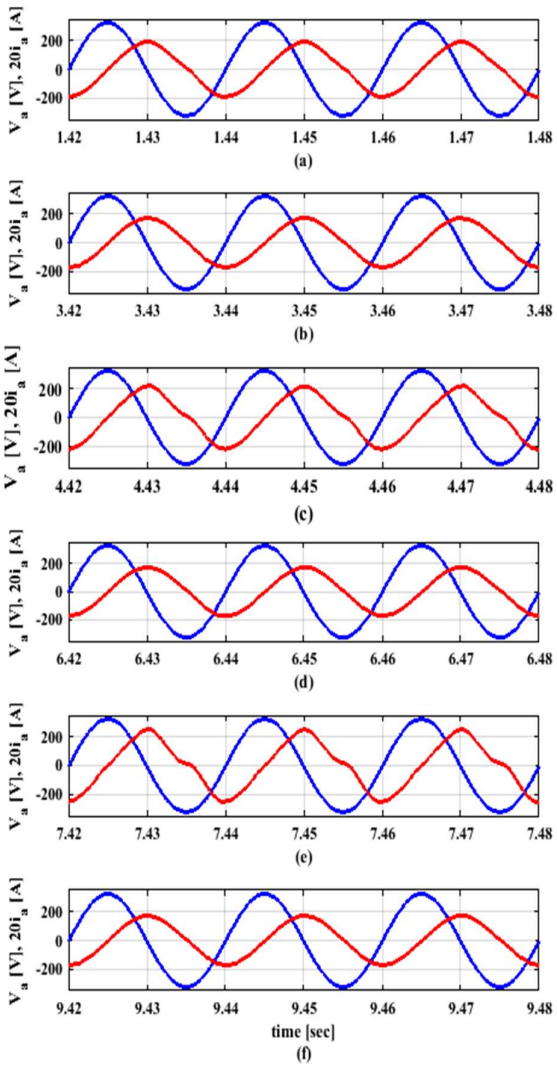


Fig. 12. Voltage and current waveforms of phase a under: (a) under 4.5 kVAr and $s_q = 1$; (b) 5 kVAr and $s_q = 0$; (c) 5 kVAr and $s_q = 1$; (d) 5 kVAr and $s_q = 0$; (e) 5.5 kVAr and $s_q = 1$; (f) 5.5 kVAr and $s_q = 0$; under faulty scenario and proposed control structure shown in Fig. 4.

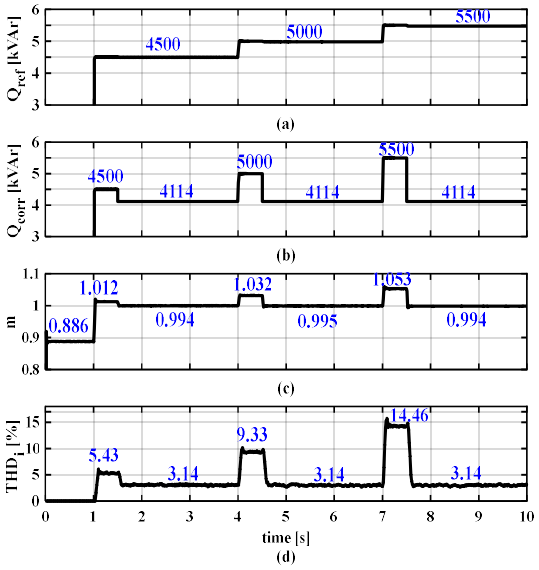


Fig. 13. (a) Original reactive power reference; (b) Corrected reactive power reference; (c) modulation index; (d) THD_i ; under faulty scenario and proposed control structure shown in Fig. 4.

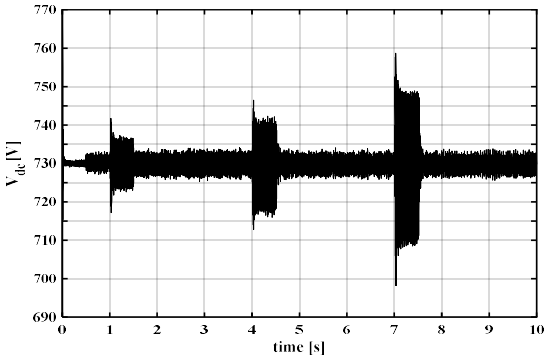


Fig. 14. DC-link voltage ripple under faulty scenario and proposed control structure shown in Fig. 4.

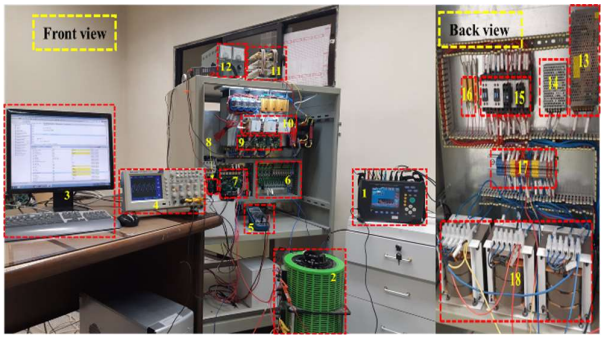
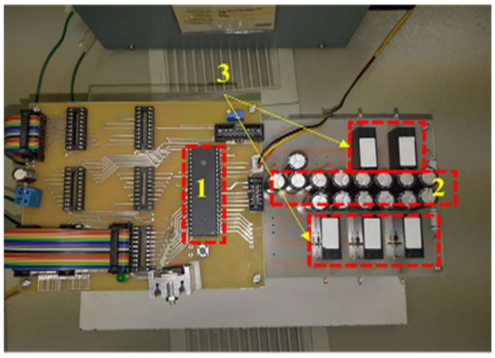


Fig. 15. Experimental setup; 1- Power Analyzer, 2- Auto transformer, 3- Code Composer Studio, 4- Scope, 5- Multi-meter, 6- Protection board, 7- Control board, 8- Digital to Analog Board, 9- Heat sink, 10- IGBT driver, 11- Capacitor bank, 12- Power supply 12VDC, 13- Power supply 12VDC, 14- Power supply 5VDC, 15- Relay contactors, 16- Pre-charge resistors, 17- Terminals, 18- Inductors

TABLE 3 Modulation index under faulty scenario

(VAr)	4500	4220	5000	4220	5500	4220
s_q	1	0	1	0	1	0
Modulation index	1.01	0.99	1.04	0.99	1.07	0.99

(a)



(b)

Fig. 16. CB circuit (a) Side view; (b) Top view: 1-ATmeaga32 Processor, 2- Capacitors, 3- Relay Contactors.

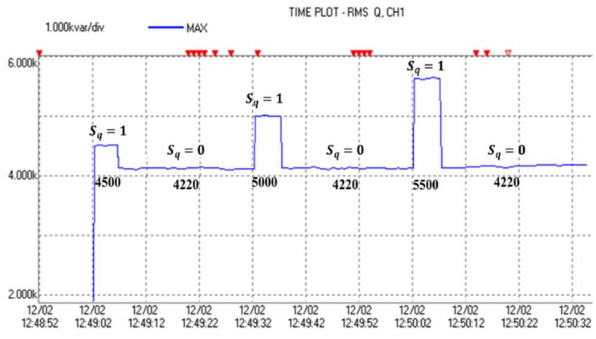


Fig. 17. Injected reactive power by d-statcom to the network at pcc

The results of the THD analysis for the injected reactive current are presented in Fig. 18. Under the under-full-load (UFL), full-load (FL), and over-full-load (OFL) compensation levels, the measured current THD values for the basic control structure shown in Fig. 2 are approximately 5.4%, 9.8%, and 13.9%, respectively. In contrast, when the proposed method starts correcting the reactive power reference, the measured THD_i is reduced to approximately 3.4%. The achieved THD values satisfy the IEEE 519 recommended limits for current distortion at the PCC.

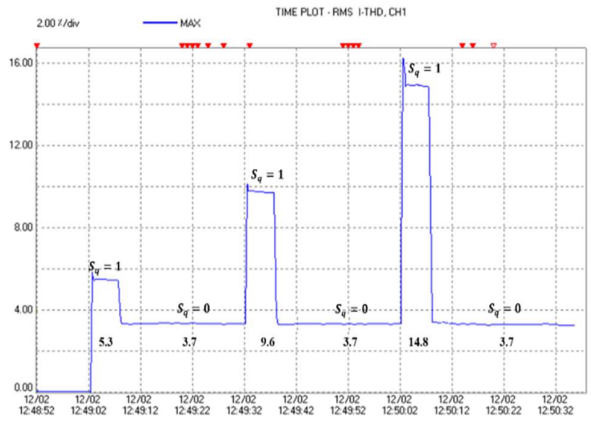


Fig. 18. THD_i profile in different compensation rates

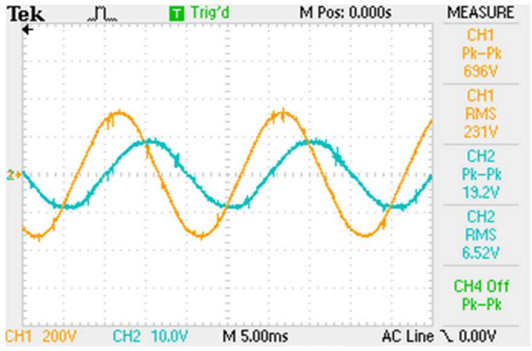


Fig. 19. Voltage and current waveform of phase a under faulty mode ($Q_{ref} = 4500$ and $s_q = 1$)

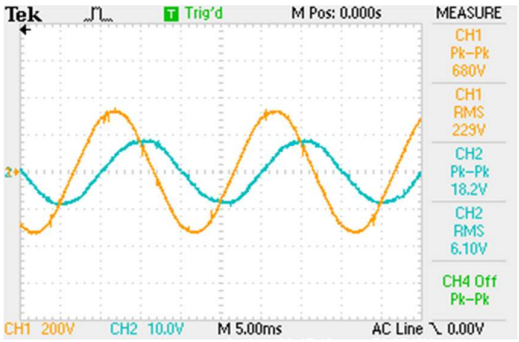


Fig. 20. Voltage and current waveform of phase a under faulty mode ($Q_{ref} = 4200$ and $s_q = 0$)

It should be noted that the time intervals associated with Scenario 2 differ slightly in the experimental results compared to the simulations, since the minimum THD measurement interval of the power quality analyzer is 1 s. The corresponding phase-a voltage and current waveforms for different operating intervals are shown in Figs. 19–22, considering various compensation levels and THD correction stages.

Under Scenario 2, the current waveforms deviate from a sinusoidal shape when the original reference is applied using the basic control system, whereas they become nearly

sinusoidal once the adaptation mechanism initiates the correction process.

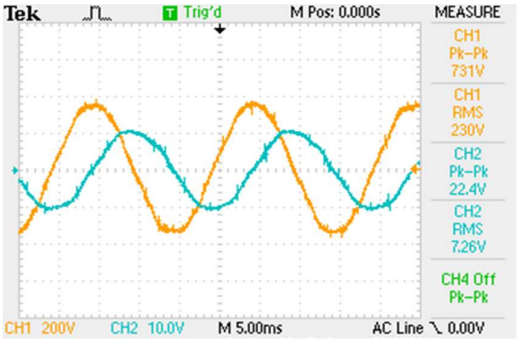


Fig. 21.Voltage and current waveform of phase a under faulty mode ($Q_{ref} = 5000$ and $s_q = 1$)

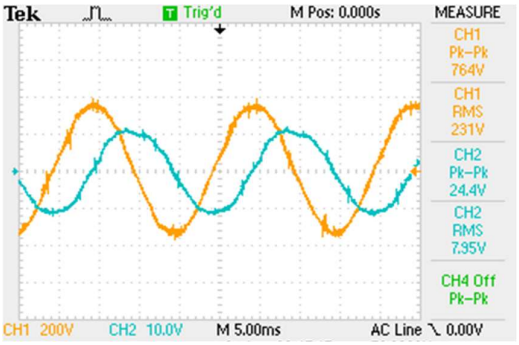


Fig. 22.Voltage and current waveform of phase a under faulty mode ($Q_{ref} = 5500$ and $s_q = 1$)

These waveform characteristics are consistent with the THD_i trends observed in Fig. 18.

Finally, the modulation index values calculated for each operating interval are summarized in Table 3. These results are in good agreement with the simulation outcomes and confirm that higher THD_i values correspond to larger modulation indices. It is also noted that the modulation index is approximately 0.88 when the D-STATCOM operates under no-load conditions.

Furthermore, since the minimum sampling interval of the THD_i, provided by the power quality analyzer is 1s, the values of $Q_{flag} = 250\ cycles$ and $THD_{flag} = 250\ cycles$ are selected in the experimental setup to clearly illustrate the different operating stages of the proposed algorithm. It should be noted that the adaptation mechanism is capable of adjusting the reactive power reference—and consequently regulating the THD—over much shorter time intervals, as demonstrated in the Simulink simulation results. Additionally, it is observed that the phase-a voltage and current waveforms are similar to those shown in Fig. 20 when $S_q = 0$ and the reactive power reference is set to $Q_{ref} = 5000$ and 5500 VAr.

In practical implementation, minor deviations may arise due to semiconductor switching dead-time, parasitic elements of the DC-link capacitor bank, relay actuation delays in the fault injection circuit, DSP sampling and computation latency, and sensor noise. Additionally, the experimental THD measurement is constrained by the power quality analyzer's 1-second evaluation window, whereas the simulation assumes ideal instantaneous computation. Despite these practical non-idealities, the steady-state trends and THD regulation performance remain consistent between simulation and experimental results, confirming the robustness of the proposed approach.

5. Conclusion

This study examined the adverse effects of DC-link capacitor bank capacitance degradation on the performance of a D-STATCOM. The analysis showed that a reduction in DC-link capacitance leads to increased DC-link voltage ripple and limitations in the modulation index, under which conventional control strategies are unable to properly regulate power quality indices—particularly the reactive current THD—resulting in degraded power quality at the point of common coupling (PCC).

To address this issue, the SAS was proposed and integrated into the existing control framework. The introduced Supplementary adaptation scheme adaptively adjusts the reactive power reference to ensure that the current THD remains within acceptable limits defined by power quality standards. Importantly, this approach does not modify the primary control loops and operates only under steady-state conditions.

During transient operating periods, the D-STATCOM continues to supply the originally demanded reactive power in order to prevent abrupt disturbances to the distribution network. The corrective action of the SAS is initiated after a predefined delay, providing sufficient time for passive compensation devices—such as switched capacitors and reactors—to supply the remaining reactive power difference $|Q_N^* - Q^*|$ that cannot be safely delivered by the D-STATCOM under THD constraints.

Both simulation and experimental results validate the effectiveness of the proposed method under DC-link capacitor bank fault conditions, where the conventional control structure exhibits inadequate THD regulation and reduced power quality. Furthermore, the results demonstrate that the SAS systematically determines the maximum admissible reactive power reference while satisfying THD limitations, achieved through concurrent reduction of the DC-link voltage ripple and the modulation index.

Future research may extend the proposed adaptation mechanism to multi-level and higher-power STATCOM topologies, investigate performance under different capacitance degradation severities, and incorporate faster or adaptive THD estimation techniques. Further analytical studies on stability margins, dynamic grid conditions, and coordination with other reactive power compensation devices would enhance the applicability of the proposed framework.

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